REMARKS

Claims 1-28 are pending. Claim 3 has been amended to correct a typographic error. The amendments to claim 3 are not for reasons of patentability. No new matter is presented.

Claims 1-4, 12-26 and 28 were rejected under 35 USC 112, first paragraph, as failing to comply with the enablement requirement. The Examiner asserts that the claims contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. This rejection is respectfully traversed.

The Examiner asserts that the "memory device" of claim 1 is not supported by the specification. Respectfully, the Examiner is mistaken. Both the specification and the drawings make numerous references to memory devices. Specifically, at pg. 9, lines 22-24, the specification states that "memories are provided before and after the color correcting unit 19 to absorb the time period for which the region discriminating process is performed at region discriminating unit 21." At pg. 10, lines 31-32, the specification states that "a memory of a necessary capacity can be mounted to each of socket A 25, socket B 27 and socket C 29." Referring to Fig. 2, sockets A, B and C can be shown and in Fig. 4, the memory devices A, B and C are shown in place (or in) the sockets A, B and C, respectively. In light of at least this disclosure, Applicant submits that one of ordinary skill in the art would be able to make and/or use the invention since the placement of the memory devices is disclosed as is the parameters of the memory devices to be used ("a memory of necessary capacity"). Applicant submits that undue experimentation would be unnecessary to make and/or use the claimed invention. Further, Applicant points out that the burden remains on the Examiner to point out why the scope of protection provided by the claim is not adequately enabled by the disclosure (see MPEP 2164.04). The Examiner has failed to meet this burden.

The Examiner next asserts that the claimed "a connecting means" is not supported by the specification. The Examiner refers to the portion of the specification at pg. 10, lines 5 and 6, and seems to be under the impression that the discussed "connecting relation between HVC converting unit 17, color correcting unit 19 and MTF correcting unit 23" corresponds to the claimed connecting

means. Applicant submits that the Examiner's impression is incorrect. Rather, the sockets A, B and C are the structures which correspond to the claimed connecting means, as can be seen in Figs. 2 and 4, and as discussed above, where the disclosure states that the memory devices are mounted to each of the sockets (pg. 10, lines 31-32). As asserted above, the specification does enable one of ordinary skill in the art to make and/or use the invention. Further, the Examiner has again failed to meet his burden under MPEP 2164.04.

The Examiner makes the same assertion with respect to the recitation of "a connecting means for" in claim 3. The remarks above with respect to claim 2 apply to claim 3 as well. Further, claim 3 has been amended to correct a typographical error. It is clear from Fig. 6 that the connecting means is arranged between the first and third processing means in the second state.

Next the Examiner asserts that "a switch device for arranging a plurality of said connecting means, corresponding to said plurality of color data, at a preceding stage of said first processing means in said first state, and for arranging said connecting means, corresponding to said one image color data, between said first processing means and said second processing means in said second state" is not supported by the specification either (citing pg. 10, lines 13-29). Claim 3 has been amended to correct a typographical error. It is clear from Fig. 6 that the connecting means is arranged between the first and third processing means in the second state. Applicant submits that the disclosure is complete and enabling to one of ordinary skill in the art. As can be seen in Figs. 2, 4 and 6, for example, the switches S1-S5 connect the sockets A, B and C to various other elements of the drawings (i.e., color correcting unit 19, etc.). The manner in which this works is further explained at pg. 10, line 13, through pg. 11, line 25. Again, Applicant is baffled as to why this disclosure is not enabling and reminds the Examiner of the burden as discussed in MPEP 2165.04 in this regard.

The Examiner's remarks with regard to the "memory device" claimed in claim 4 are discussed above in connection with the discussion of the recitation of the memory device in claim 1.

Regarding claim 12, the Examiner asserts that the limitation "said third processing unit substantially simultaneously receives the image data from said first processing unit and data corresponding to said image data from said second processing unit" is not supported by the specification "at all." Again, the Examiner is mistaken. The specification clearly describes that in the MTF correcting unit 23 (corresponding to the claimed third processing unit), the timing at which the image color data of CMYK are received from color correcting unit 19 (corresponding to the first processing unit) and the timing at which the attribute data is received from region discriminating unit 21 (corresponds to claimed second processing unit) are synchronized (pg. 9, lines 19-22). Thus, this limitation is indeed supported by the specification.

Regarding claim 13, the Examiner asserts that the claimed first circuit, second circuit, and switch device are not supported by the specification as cited on pg. 9, lines 22-24. Applicants believe this has been addressed above, but submit that these limitations are clearly supported by the specification as seen in Figs. 6 and 7 and the corresponding descriptions (see, for example, pg. 16, line 28 to pg. 17, line 6).

Regarding claim 20, the Examiner asserts that the limitations "a first circuit to input image data including a set of a plurality of color data output from said memory device into said first processing unit; a second circuit to input one image color data output from said first processing unit into said memory device, and also inputting one image color data output from said memory device into said second processing unit; and a switch device to selectively switch said first circuit and said second circuit to select said first circuit in said first state and to select said second circuit in said second state" are not supported by the specification. In light of the remarks regarding claim 13, Applicant submits that these features are indeed supported by the specification.

The rejection of claim 28 is similar to the rejection of claims 13 and 20 and is traversed for the same reasons. In light of the foregoing remarks, Applicant requests that this rejection be withdrawn.

Claims 1-11 and 27 were rejected under 35 USC 102(e) as being anticipated by Yoshida, U.S. Patent 6,538,769. This rejection is respectfully traversed.

Claim 1 recites "a first processing means for sequentially processing input pixel data; a memory device provided at a preceding stage of said first processing means to store said pixel data; a second processing means for determining a characteristic of an image region including a plurality of said pixel data." According to claim 1, the data to be input to the first processing means and data to be input to the second processing means is the same pixel data. This is not the case in Yoshida. The Examiner asserts that the HVC conversion unit 125 corresponds to the claimed first processing means and that the area discrimination unit 144 corresponds to the claimed second processing means. In this case, the HVC conversion unit 125 converts the R, G, B image data into value signals and coloring signals, but this pixel data is not the same data which is input to the area discrimination unit 144.

Furthermore, according to claim 1, the memory device is provided at a preceding stage of the first processing means to store pixel data. The Examiner asserts that the inter-line correction unit 123 corresponds to the claimed memory device. However, merely because the inter-line correction unit contains a memory, does not mean that these devices perform the same function. The inter-line correction unit does not store the pixel data, but rather performs line unit data delay suited to the scan speed (col. 4, lines 16-18). Accordingly, the features of claim 1 are not taught or suggested by Yoshida.

Claims 4 and 27 are allowable for the same reasons claim 1 is allowable.

Claim 2 recites "a switch device for switching a circuit such that said connecting means is arranged either at a preceding stage of said first processing means or between said first processing means and said third processing means." The Examiner asserts that selector 112/113 corresponds to the claimed switch. However, the selector does not switch the circuit such that the connecting means is arranged either at a preceding stage of the first processing means or between the first processing means and the third processing means. The selector of Yoshida is not capable of

rearranging the placement of the memory. Regardless of whether the Examiner believes that Applicant has established "a clear relationship between the connecting means and the switch as being a combined function," the fact remains that the claimed switch device enables the placement of the memory device to be changed from either before the first processing means or between the first processing means and the third processing means. Yoshida fails to teach or suggest this feature. The features of claim 2 are not taught or suggested by Yoshida.

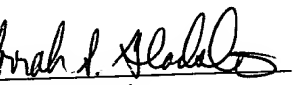
Claim 3 is allowable for the same reason claim 2 is allowable. Claims 5-11 are allowable at least due to their respective dependencies. Accordingly, Applicant requests that this rejection be withdrawn.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue. If it is determined that a telephone conference would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at the number given below.

In the event the U.S. Patent and Trademark office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to Deposit Account No. 03-1952 referencing docket no. 325772023600.

Dated: February 24, 2005

Respectfully submitted,

By 

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